REMARKS

Claims 1-22 are pending in the present application.

In the office action mailed April 26, 2005 (the "Office Action"), the Examiner objected to the drawings and further objected to claims 1, 4, 9, and 13-16, based on informalities. The Examiner also rejected claims 1-22 under 35 U.S.C. 112, second paragraph.

With respect to the Examiner's objections to the drawings, Figures 3 and 5 have been amended as suggested by the Examiner. Additionally, the specification has been amended to remove reference to the "discharge controller 300." As for the Examiner's objection to the drawings for failing to show "an input signal" and "a test signal," Figure 4 illustrates an input signal and a test signal. In the embodiment illustrated in Figure 4, the input signal is generated at the node 514 by the PMOS and NMOS transistors 510, 512. The input signal at the node 514 has a HIGH logic level in response to the VXDECEN# and XPDA signals having LOW logic levels. Conversely, when the VCDECEN# and XPDA signals have HIGH logic levels, the input signal at the node 514 has a LOW logic level. Operation of the row driver 500 in response to the input signal at the node 514 and the VXDECEN# and XPDA signals is described at page 7, line 23-page 8, line 17. In the embodiment of the row driver shown in Figure 4, the test signal corresponds to the PSM signal that is provided to the isolation circuit 502. As described in the present application, the PSM signal indicates whether a flash memory is operating in a normal mode or in a power-savings mode. See page 7, lines 20-21. Operation of row driver 500 with respect to the PSM signal is described at page 7, line 23-page 8, line 17. Thus, both "an input signal" and "a test signal" are shown in Figure 4. For the foregoing reasons, the Examiner's objections to the drawings should now be withdrawn.

Claims 1, 4, 9, and 13-16 have been amended as suggested by the Examiner to overcome the Examiner's objections to these claims. Consequently, the Examiner's objection to claims 1, 4, 9, and 13-16 should now be withdrawn.

As previously mentioned, claims 1-22 have been rejected under 35 U.S.C. 112, second paragraph.

The Examiner has rejected claims 1, 7, 11, and 14 as being indefinite due to the use of the term "an input signal," and has rejected claims 1, 7, 11, 14, 17, and 20 as being indefinite due to the use of the term "a test mode signal." As previously discussed with the

Examiner's objection to the drawings, the specification describes and the drawings illustrate an embodiment of a row driver that includes an input signal and a test mode signal. Although every term used in a claim should be apparent from the descriptive portion of the specification, it is also true there is no requirement that the words in the claim must match those used in the specification disclosure. See MPEP 2173.05(e). Although not described using the identical terms found in the claims, the description of the operation of the conventional row driver 200 and the operation of the row driver 500 in the present application provide sufficient clarity to identify an example of an input signal that is generated at the nodes 212 and 514, and an example of the test mode signal that is provided by the PSM signal. More specifically, the nodes 212 and 514 at which the input signals are generated for the conventional row driver 200 and the row driver 500, are illustrated in Figures 2 and 4, and the use of the PSM signal as the test mode signal is also illustrated in Figure 4. Consequently, the terms "an input signal" and "a test mode signal" are sufficiently definite to particularly point out and distinctly claim the subject matter regarded as the claimed invention.

Claims 17 and 20 have been rejected as being indefinite for using the term "a row activation signal." The specification has been amended to provide clear disclosure of the term in the specification.

With respect to the double inclusion of the terms "input signal," "test mode signal," and "high impedance," claim 4 has been amended to clarify that the terms refer to the same "input signal," "test mode signal," and "high impedance."

With respect to the reference of "the first signal terminal" and "the second signal terminal" in claim 4, claim 4 has been amended to remove the use of "signal," as recommended by the Examiner. Additionally, claim 4 has been further amended to make reference to "a reference voltage" to address the lack of antecedent basis.

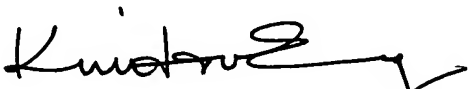
Claim 14 has been amended to remove "signal" from "the first and second signal terminals," and to reference "a reference voltage" to address the lack of antecedent basis.

Finally, with respect to the Examiner's recommendation to remove the phrase "adapted to" from the claims, the undersigned does not agree that the phrase "adapted to" will be interpreted as characterized by the Examiner. Consequently, the phrase "adapted to" has not been removed from the claims.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Kimton N. Eng
Registration No. 43,605
Telephone No. (206) 903-8718

KNE:ajs

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 3 and 5.

Figure 3 has been amended so that the gate-induced drain leakage is labeled in Figure 3 as "IGIDL".

Figure 5 has been amended to correct a typographical error in circuit block 464, to remove an arrow pointing to WSM 406, to remove an arrow pointing to the I/O Logic 412, and to remove "the third arrow pointing to the right bottom side of circuit block 448a".

Enclosed are 4 sheets of replacement formal drawings, Figures 1-6, for filing in the above-identified application.

Attachments: Annotated Sheets Showing Changes
Replacement Sheets

Annotated Sheet
Showing Changes

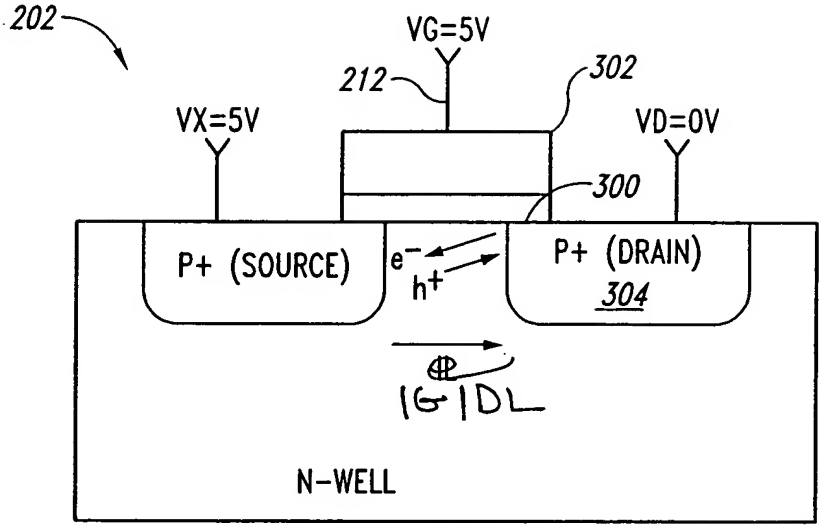

Fig. 3
(Background Art)

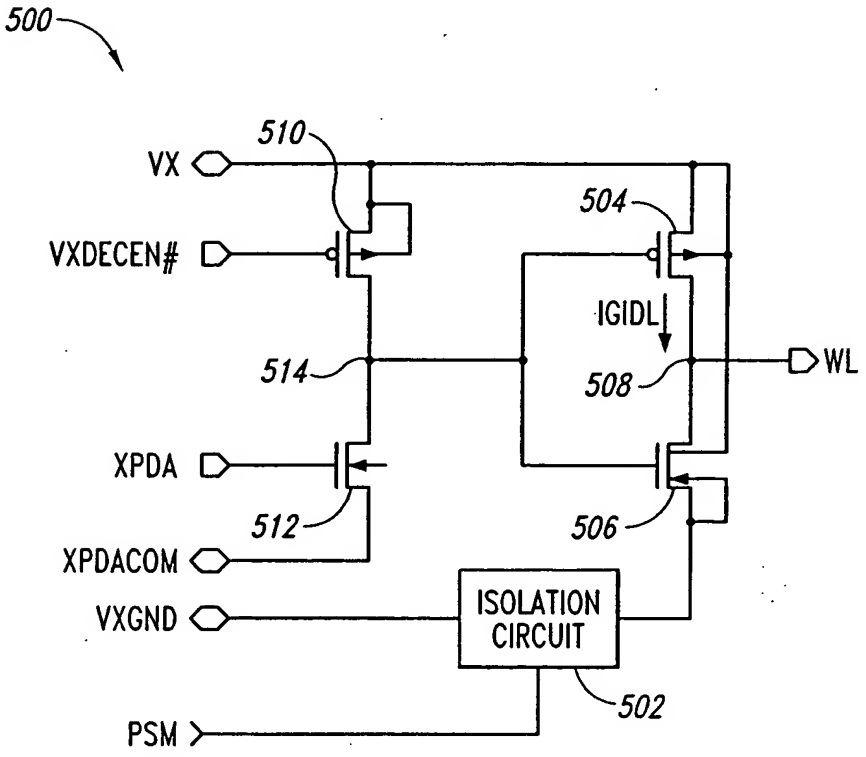

Fig. 4

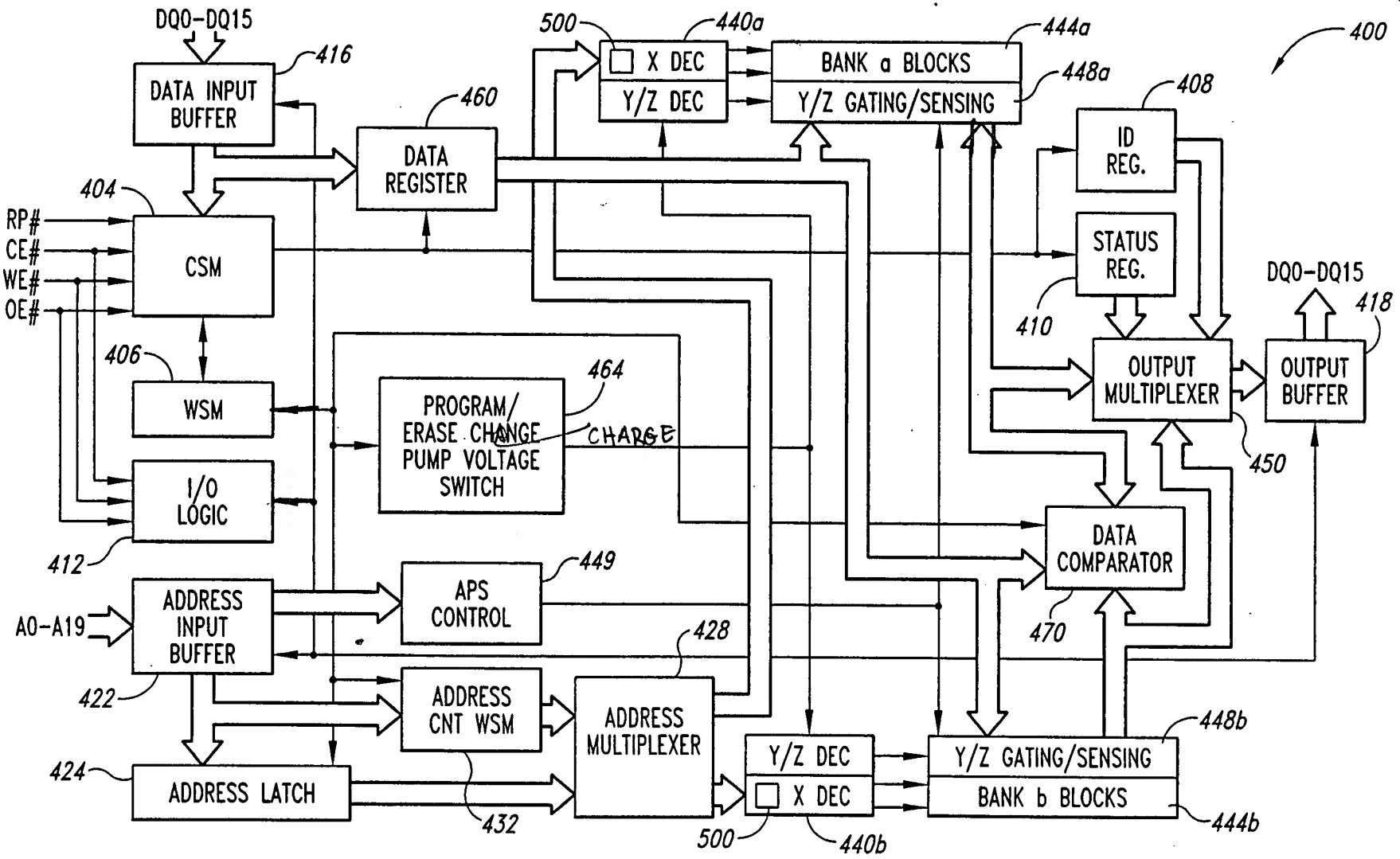

Fig. 5

Annotated Sheet Showing Changes